Course Code: 20EC4209 **R20**

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
Siddharth Nagar, Narayanavanam Road – 517583
QUESTION BANK (DESCRIPTIVE)

Subject with Code: FPGA ARCHITECTURES & APPLICATIONS (20EC4209)
Course & Branch: M.Tech-VLSI
Regulation: R20 **Year & Sem:** I-M.Tech & II-Sem

UNIT –I

PROGRAMMABLE LOGIC

1	a)	Draw the structure of PAL and explain it.	[L1][CO1]	**[6M]**
	b)	Draw the logic diagram of MAX 7000 CPLD macrocell and explain its Functioning.	[L1][CO1]	**[6M]**
2	a)	Draw the structure of PLA and explain it.	[L2][CO1]	**[6M]**
	b)	Explain the LAB of Altera max 7000 CPLD with a neat structural diagram.	[L1][CO1]	**[6M]**
3	a)	Implement the following Boolean function using PLA having 3 inputs, 3product terms and 2 outputs. $F_1(A,B,C) = AB'C' + AB'C + ABC$ $F_2(A,B,C) = A'BC + AB'C + ABC$	[L3][CO1]	**[6M]**
	b)	Explain Cypress FLAH 370 family of CPLDs.	[L2][CO1]	**[6M]**
4	a)	Compare PLA, PAL and PLDs with respect to different features, programming and Applications.	[L4][CO1]	**[6M]**
	b)	Explain and draw the architecture of lattice ISPLSI CPLD.	[L2][CO1]	**[6M]**
5	a)	Explain and draw the architecture of AMD Mach 4 CPLD.	[L2][CO1]	**[6M]**
	b)	Explain the architecture of Altera Max 7000 series.	[L2][CO1]	**[6M]**
6	a)	Explain the ROM Organisation with neat diagrams.	[L2][CO1]	**[6M]**
	b)	Discuss about speed performance and in-system programmability of lattice PLST's architecture in 3000 series.	[L2][CO1]	**[6M]**
7	a)	Implement the circuit with a PLA having 3 inputs, 4 product terms, and 2 outputs. $F_1 = A'BC + AB'C + ABC' + ABC$; $F_2 = A'B'C' + AB'C' + A'BC' + ABC$	[L3][CO1]	**[6M]**
	b)	Implement the following Boolean function using PLA: $F_1(w, x, y, z) = \Sigma m (0, 2, 4, 6, 8, 10, 11, 12, 14, 15)$ $F_1(w, x, y, z) = \Sigma m (0, 2, 4, 6, 8, 10, 11, 12, 14, 15)$	[L3][CO1]	**[6M]**
8	a)	Compare the salient features of AMD's CPLD Mach 1 to 5.	[L4][CO1]	**[6M]**
	b)	Implement the following Boolean function using PAL: $F(w, x, y, z) = \Sigma m (0, 2, 4, 6, 8, 10, 11, 12, 14, 15)$	[L3][CO1]	**[6M]**
9	a)	Distinguish between FPGA and CPLD.	[L2][CO1]	**[6M]**
	b)	Implement the following Boolean function using PLA: $F_1(w, x, y, z) = \Sigma m (0, 2, 4, 6, 8, 10, 11, 12, 14, 15)$ $F_1(w, x, y, z) = \Sigma m (0, 2, 4, 6, 8, 10, 11, 12, 14, 15)$	[L3][CO1]	**[6M]**
10	a)	Explain the different types of ROMs.	[L2][CO1]	**[6M]**
	b)	Design the following function using ROMs. $F=XYZ^I+Y^I Z+X\ ^I Y^I$	[L2][CO1]	**[6M]**

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UNIT –II
FPGA

1	a)	Write about FPGA Programming Technologies in detail.	[L1][CO2]	**[6M]**
	b)	What is an FPGA ? Mention the advantages & disadvantages of FPGA.	[L1][CO2]	**[6M]**
2	a)	Draw the architecture of Altera flex 8000 FPGAs and Explain it.	[L1][CO6]	**[6M]**
	b)	Draw the structure of Actel FPGAs and explain it.	[L1][CO2]	**[6M]**
3	a)	Explain the functions of different blocks in Xilinx XC4000 CLB.	[L2][CO6]	**[6M]**
	b)	Draw the design flow of field programmable gate arrays.	[L1][CO2]	**[6M]**
4	a)	Draw and explain the routing architecture of field programmable gate arrays	[L1][CO2]	**[6M]**
	b)	Explain the architecture and speed performance of Actel's ACT2 FPGA family.	[L2][CO2]	**[6M]**
5	a)	Draw the architecture of Altera flex 10000 FPGAs and Explain it.	[L1][CO6]	**[6M]**
	b)	List out the applications of FPGAs.	[L4][CO1]	**[6M]**
6	a)	Describe Technology Mapping for FPGAs.	[L2][CO6]	**[6M]**
	b)	Explain the AT&T ORCA FPGAs.	[L2][CO6]	**[6M]**
7	a)	Write about programmable I/O blocks in FPGA.	[L1][CO2]	**[6M]**
	b)	Compare the performance parameters of ACTEL based FPGAs ACT-1,2 and 3 .	[L4][CO2]	**[6M]**
8	a)	Draw and explain the CLB and IO Blocks of Xilinx XC4000 architecture.	[L1][CO6]	**[6M]**
	b)	Explain about different programmable elements in FPGA architectures.	[L2][CO2]	**[6M]**
9	How the ACT3 architecture is different from ACT2 architecture? Explain the ACT3 architecture in detail.		[L1][CO2]	**[12M]**
10	a)	Explain the ACT1 architecture for high fan-in example.	[L2][CO2]	**[6M]**
	b)	Compare the speed performance of ACT 1,2,3.	[L4][CO2]	**[6M]**

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UNIT –III
Finite State Machines (FSM)

1	a)	Explain about FSM types, properties, design and applications.	[L2][CO3]	**[6M]**
	b)	Explain about state assignments for FPGA.	[L2][CO3]	**[6M]**
2	Discuss the problem of Initial state assignment for one hot encoding.		[L2][CO3]	**[12M]**
3	a)	Explain the basic concepts of petrinets and state its properities	[L2][CO3]	**[6M]**
	b)	Write about linked state machine.	[L1][CO3]	**[6M]**
4	a)	Describe about alternative realisaztion for state machine chart using microprogramming.	[L2][CO3]	**[6M]**
	b)	Explain about realization for state machine charts with a PAL.	[L2][CO3]	**[6M]**
5	a)	Illustrate about metastability characteristics.	[L3][CO3]	**[6M]**
	b)	Discuss about Extended Petri nets for Parallel Controllers.	[L2][CO3]	**[6M]**
6	a)	What is state transition table? Explain how state assignment can be carried for FPGA.	[L1][CO3]	**[6M]**
	b)	Explain Derivations of state machine charges.	[L2][CO3]	**[6M]**
7	Explain about one hot state machine and give one example		[L2][CO3]	**[12M]**
8	a)	What is state diagram and explain with examples.	[L1][CO3]	**[6M]**
	b)	Explain the structure of petrinets.	[L2][CO3]	**[6M]**
9	a)	Explain about Finite state machine case study.	[L2][CO3]	**[6M]**
	b)	Illustrate about synchronization.	[L2][CO3]	**[6M]**
10	a)	Write the significance of FSM.	[L1][CO3]	**[6M]**
	b)	Determine the derivations of SM Chart.	[L6][CO3]	**[6M]**

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UNIT –IV
FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN

1	a)	Explain about non-Registered PLDs.	[L2][CO4]	**[6M]**
	b)	Design of the one to three pulse generator by using PLA.	[L5][CO4]	**[6M]**
2	a)	Design of the one to three pulse generator by using ROM.	[L5][CO4]	**[6M]**
	b)	Design of a More Complex FSM by using a ROM as the PLD.	[L5][CO4]	**[6M]**
3	a)	What is state machine? Explain about state machine applications.	[L1][CO4]	**[6M]**
	b)	Explain about state machine types.	[L2][CO4]	**[6M]**
4	a)	Explain state machine theory and implement the state diagram representation.	[L2][CO4]	**[6M]**
	b)	Explain about state transition table.	[L2][CO4]	**[6M]**
5	a)	Classify the state machine types.	[L3][CO4]	**[6M]**
	b)	Discuss the device selection consideration.	[L2][CO4]	**[6M]**
6	a)	Design a one- hot controller for the ASM.	[L5][CO4]	**[6M]**
	b)	Explain one - hot technique in FSM design.	[L2][CO4]	**[6M]**
7	a)	Design the one - hot version of the single pulse FSM.	[L5][CO4]	**[6M]**
	b)	Describe the ASM and explain one example.	[L2][CO4]	**[6M]**
8	a)	Design a serial bit clock by using ASM.	[L5][CO4]	**[6M]**
	b)	List and explain the applications of one - hot method.	[L4][CO4]	**[6M]**
9	Explain about system level design by using controller.		[L2][CO4]	**[12M]**
10	a)	Explain the data path devices in system level design.	[L2][CO4]	**[6M]**
	b)	Discuss the functional partition in system level design.	[L2][CO4]	**[6M]**

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UNIT –V
CASE STUDIES

1	Design the CLB combinational circuit by using parallel adder cell.	[L5][CO5]	**[12M]**
2	Design the Schematic for full adder combinational circuit by using parallel adder cell.	[L5][CO5]	**[12M]**
3	Design the combinational circuit by using parallel adder.	[L5][CO5]	**[12M]**
4	Design a decade counter and explain the process of implementing their design on FPGAs.	[L5][CO5]	**[12M]**
5	Design the state machine for decade counter.	[L5][CO5]	**[12M]**
6	Explain the Macro cell for 74610 decade counter.	[L2][CO5]	**[12M]**
7	Design the parallel combinational logic multiplier with example.	[L5][CO5]	**[12M]**
8	Design the serial multiplier with parallel addition.	[L5][CO5]	**[12M]**
9	Discuss about a parallel controller design.	[L5][CO5]	**[12M]**
10	Explain the operation of part of the petri net controller.	[L2][CO5]	**[12M]**

Prepared by: M.Shobha